Questa Advanced Simulator on HPC

What is Questa Advanced Simulator?

Questa Advanced Simulator is a high-performance, highly-accurate simulation tool for use in the design and verification of digital electronic systems. It is developed and distributed by Mentor, a Siemens Business, as part of the Questa Platform for functional verification.

Questa Advanced Simulator supports a wide range of design languages and standards, including VHDL, Verilog, SystemVerilog, and SystemC. It can be used to simulate large and complex designs, including ASICs and FPGAs, at various levels of abstraction, from gate-level to transaction-level. It includes a variety of advanced features and technologies to improve simulation speed and accuracy, such as multi-threading, distributed simulation, and hybrid simulation.

In addition to simulation, Questa Advanced Simulator also includes a range of debugging and visualization tools to help users analyze and understand the behavior of their designs. It can be used in conjunction with other tools in the Questa Platform, such as Questa Formal, for formal verification, and Questa Verification IP, for verification of standard IP blocks.

Links:

Official Website

Versions Available:

The following versions are available on the cluster:

- Questa Advanced Simulator v10.6d

How to load Questa Advanced Simulator?

To load QUESTA ADVANCED SIMULATOR, use the following commands:

```
#Load the  Questa Advanced Simulator module
module load questasim/10.6d
```

To verify if the module and dependencies are loaded correctly, use the following command.

```
#Show all the modules loaded
module list
```

This should list all the QUESTA ADVANCED SIMULATOR dependencies that are loaded – only questasim.

```
Note: All the documentation of the software is available in the
following directory location -
/share/apps/Mentor_Graphics/questasim/docs
```

How to use Questa Advanced Simulator?

To use Questa GUI, user need to jump into a compute node by using following command,

```
#Jump to compute node after loading necessary module
srun -p main --qos main -n 1 -c 16  --mem 16G --pty vsim
```

Note: User need to login with X11 forwarding

```
# Log in using this command to activate X11 forwarding
ssh -X bigal@uahpc.ua.edu
```

To see all the command line arguments for the, use the following command

```
# Command line args
vsim -h
```

Prepare your input files: Questa Advanced Simulator requires several input files to specify the design you want to simulate, including a design file written in a hardware description language

(HDL) such as VHDL or Verilog, and any necessary testbench or stimulus files. Make sure you have all of the necessary input files available.

Use the following sample slurm script for reference.

```
#!/bin/bash

#SBATCH --job-name=questa_sim
#SBATCH --output=questa_sim.out
#SBATCH --error=questa_sim.err
#SBATCH -p main
#SBATCH --qos main
#SBATCH --nodes=1
#SBATCH --cpus-per-task=16
#SBATCH --time=24:00:00
#SBATCH --mem=16GB

# load necessary modules
module load questasim/10.6d


# run Questa Advanced Simulator
vsim -c -do "run -all; quit" -l questa_sim.log design_top
```

See the documentation for more information about this software.

Where to find help?

If you are confused or need help at any point, please contact OIT at the following address.

https://ua-app01.ua.edu/researchComputingPortal/public/oitHelp